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(54) Process for making structures including E2PROM nonvolatile memory cells with self-aligned layers of silicon and associated transistors.

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EP-A- 0 112 078
DE-A- 3 106 202
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Description

The present invention relates to a process for making structures including E^2PROM nonvolatile memory cells with self-aligned layers of silicon and associated transistors.

An E^2PROM nonvolatile memory cell is known to comprise a floating gate of polycrystalline silicon superimposed on a layer of gate oxide superimposed in turn on a substrate of monocrystalline silicon appropriately doped and a control gate of polycrystalline silicon in turn superimposed on the floating gate and insulated electrically from the latter by a thin layer of silicon oxide.

With the cell is associated a selection transistor formed of two superimposed uninsulated layers of polycrystalline silicon placed over the gate oxide.

Also usually present are similarly formed transistors which are part of the external circuitry.

The abovesaid cells can be made with better optimization of the area used if there is applied a technology permitting self-aligning of the floating and control gates. In this case all the silicon area of the control gate can be used for capacitive coupling of the floating and control gates, optimizing the writing and cancellation operations of the cell.

A known technique for making memory cells with self-aligned layers of polycrystalline silicon and associated selection and circuitry transistors calls for the following sequence of operations: (a) deposit of a first layer of polycrystalline silicon on a substrate of monocrystalline silicon furnished in advance with field oxide and gate oxide, (b) definition and etching of said first silicon layer, (c) growth of a thin layer of oxide on said first silicon layer, (d) etching of said oxide layer over the entire area intended for formation of the transistors, (e) deposit of a second layer of polycrystalline silicon and (f) final etching of the two layers of polycrystalline silicon and of the intermediate oxide layer outside the zones intended for formation of the memory cell and transistors.

In this manner there is obtained a resulting structure including one or more memory cells having two self-aligned layers of polycrystalline silicon with interposed oxide and associated selection and circuitry transistors with two self-aligned and short-circuited layers of polycrystalline silicon.

This manufacturing technique displays possible criticality with regard to the final etching of the two layers of silicon and the intermediate oxide. If the first etching step of the second silicon layer is continued until the gate oxide is reached in the regions without intermediate oxide, there occurs during the etching steps of the intermediate oxide and of the first silicon layer an undesirable excavation of the monocrystalline silicon substrate.

To obviate this inconvenience there has been proposed a process variant which calls for stopping the etching of the second silicon layer before it uncovers the gate oxide, thus leaving part of the first silicon layer protecting the latter in the regions having shortcircuited silicon. The subsequent etching of the intermediate oxide and of the first oxide layer thus takes place without excavation of the substrate.

This solution requires however the availability of a refined etching technology permitting sizing of the necessary overetchings.

From US-A-4766088 is known a process for making a gate structure for a memory cell transistor comprising :

a) depositing a first layer of polycrystalline silicon on a substrate of monocrystalline silicon furnished in advance with field oxide and gate oxide;

b) defining and etching of said first polycrystalline layer;

c) growth of a thin intermediate layer of oxide on said first silicon layer;

d) etching a window in the intermediate oxide layer, said window being narrower than the desired width of the gate structure;

e) blanket deposition of a second layer of polycrystalline silicon; and

f) final etching of the two polysilicon layers and of the intermediate oxide layer using a mask formed in such a manner as to superimpose on the second silicon layer, at least in the memory transistor area, a covering wider than the corresponding window in the intermediate oxide layer.

GB-A-2081012 discloses a method for manufacturing a nonvolatile semiconductor memory device in which the control gate extends beyond the edges of the underlying floating gate.

In view of this state of the art the object of the present invention is to develop a process for the manufacture of gate structures for E^2PROM memory cells with self-aligned silicon layers and associated selection and circuitry transistors, which is free of the aforesaid drawbacks.

In accordance with the invention said object is achieved by a process as defined in claim 1.

In this manner, i.e. by creating between the mask in the transistor zone and the edges of the oxide layer at the sides of the related window a partial superimposition which of course must be greater than the alignment tolerance of the exposure machine used, it is possible to offer to the final etching in the unprotected zones the same combinations of layers to be etched. This avoids the drawbacks of the known art and simplifies the etching technology itself, protecting from overetching the monocrystalline silicon of the substrate.

The annexed drawings illustrate the following :
FIGS. 1-5 show the various operational steps of a prior art process,
FIGS. 6-10 show the operational steps of the process in accordance with the invention, and
FIGS. 11-14 show the operational steps of a process not forming part of the invention.

The prior art process illustrated in FIGS. 1-5 provides that on a substrate 1 of monocrystalline silicon having field oxide areas 2 and a thin layer of gate oxide 3 there is initially deposited a first layer 4 of polycrystalline silicon (FIG. 1).

By appropriate resist masking there is subsequently performed etching and the resulting removal of the silicon layer 4 corresponding to the oxide areas 2. On the residual layer there is then grown a thin layer of silicon oxide 5 (FIG. 2).

By employing suitable resist masking 6 having windows 7 and 8 there is subsequently performed etching of the oxide 5 in which there are opened small windows 9 and 10 in the zones intended for formation of the selection and circuitry transistors (FIG. 3).

The resist 6 is then removed and there is deposited a second poycrystalline silicon layer 11 on which is applied another resist masking made up of three areas 12, 13 and 14 the position and width of which correspond to the position and width desired for the memory cell and the selection and circuitry transistors. As may be seen from FIG. 4 the resist coverings 13 and 14 are wider than the corresponding windows 9 and 10 made in the oxide 5. The overlap of said coverings 13 and 14 in relation to the oxide layer 5 is at least equal to the alignment tolerance due to the exposure machine used.

Final etching is then performed of the double silicon layer 4 and 11 and of the intermediate oxide 5 performed with a first etching step of the top silicon layer 11 and a second etching step of the oxide 5 and of the bottom layer of silicon 4.

As it meets layers of the same composition the etching originates uniform removal of material at the sides of the cell area 15, of the selection transistor 16 and of the circuitry transistor 17 as shown in FIG. 5.

The process illustrated in FIGS. 1-5 has the drawback of not providing the components of minimal dimensions provided by photolithographic technology. Indeed, the minimum width of the components is determined by the minimum aperture 7, 8 allowed by the lithographic process used and by the etchings, plus twice the alignment tolerance and an additional margin due to the dimension control tolerance of the strip of polycrystal to be defined.

According to the current invention, this limitation can be eliminated for the peripheral circuitry (transistor 17) by appropriate masking. More precisely, as shown in FIG. 6 the structure of FIG. 2 is coverd with a resist mask 18 which leaves uncovered a small area 19 in the zone intended for the selection transistor 16 as well as the entire area intended for the circuitry transistor 17. The oxide layer 5 is then removed in a small area 20 underlying the open area 19 of the resist 18 and over the entire area of the circuitry transistor 17.

Once the resist 18 has been removed there is deposited the second silicon layer 11 on which is grown a second oxide layer 21. On the resulting structure (FIG. 7) there is applied another resist masking formed again of three areas 12, 13 and 14 like those illustrated in FIG. 4. In this case too the resist covering 13 is wider than the underlying window 20 of oxide 5, the overlap being at least equal to the alignment tolerance of the exposure machine used.

There follows a first step of etching of the second oxide layer 21, of the second silicon layer 11 and of the first oxide layer 5 stopping at a point corresponding to the first silicon layer 4 as concerns the cell and selection transistor areas. Lacking the protection of the oxide 5 the etching continues up to the gate oxide 3 at the sides of the circuitry transistor area (FIG. 8).

The resist 12, 13 and 14 is then removed and on the circuitry area 17 is applied another resist mask 22 (FIG. 9).

Finally the etching is completed at the sides of the cell area 15 and the selection transistor area 16 until there is obtained the final result shown in FIG. 10 after removal of the mask 22. In this last step the second oxide layer 21 is used as a mask for the cell 15 and the transistor 16.

As another alternative, not claimed, if it is desired to save the second oxide layer 21, the process could use in place of the mask 12, 13, 14 of FIG. 7, after the step shown in FIG. 6 and subsequent deposit of the second silicon layer 11, the mask illustrated in FIG. 11, which is composed of a single segment 23 on the cell and selection transistor areas and of a small segment 24 on the circuitry transistor area.

Etching is then performed of the two silicon areas 11 and 4 and of the gate oxide 3 in the unprotected intermediate area (FIG. 12).

After removal of the resist 23, 24 there is applied another masking 25, 26 and 27 of which the part 26 is again wider than the underlying oxide window 20. The part 27 covers in turn the entire area of the circuitry transistor (FIG. 13) including the adjacent uncovered zones of monocrystalline silicon (30).

Finally the final etching, before the top layer of silicon 11 and oxide 5 (FIG. 13) at the sides of the protected zones and then of the bottom layer of

silicon 4, leads to the final result shown in FIG. 14.

Claims

1. Process for manufacturing gate structures for a selection MOS transistor of an EEPROM non-volatile memory cell with self-aligned polysilicon layers and an associated circuitry transistor, comprising the following succession of steps:
   a) deposit of a first layer (4) of polycrystalline silicon on a substrate (1) of monocrystalline silicon previously provided with field oxide areas (2) and a gate oxide layer (3);
   b) definition and etching removal of said first polysilicon layer (4) on said field oxide areas (2);
   c) growth of a thin oxide layer (5) on said first polysilicon layer (4);
   d) etching removal of said thin oxide layer (5) to form a a window (20) in an area (16) intended for formation of the selection transistor, said window (20) being narrower than the desired width of the gate structure of the selection transistor, and etching removal of said thin oxide layer over the entire area of the circuitry transistor;
   e) deposit of a second layer (11) of polycrystalline silicon over the entire structure;
   f) deposit of a further oxide layer (21) over said second polysilicon layer (11);
   g) application of a mask (12, 13, 14) on said further oxide layer (21) to cover areas (15, 16, 17) for formation of the memory cell and the selection and circuitry transistors, the selection transistor area (16) including said window (9);
   h) etching removal of the further oxide layer (21), the second polysilicon layer (11) and the thin oxide layer (5) at the sides of said memory cell and selection transistor areas (15, 16) and of the further oxide layer (21), the first and second polysilicon layers (4, 11) and the gate oxide layer (3) at the sides of said circuitry transistor area (17) so as to define a circuitry transistor gate structure (17) formed by portions of said gate oxide layer (3), said first and second polysilicon layers (4, 11) and said further oxide layer (21);
   i) replacement of said mask (12, 13, 14) with a further mask (22) covering the circuitry transistor area (17);
   j) etching removal of the first polysilicon layer (4) at the sides of the memory cell and selection transistor areas (15, 16) so as to define a memory cell gate structure (15) formed by portions of said gate oxide layer (3), said first polysilicon layer (4), said thin oxide layer (5), said second polysilicon layer (11) and said further oxide layer (21) and a selection transistor gate structure (16) formed by portions of said gate oxide layer (3), said first polysilicon layer (4), said thin oxide layer (5) with said window (20), said second polysilicon layer (11) and said further oxide layer (21).

Patentansprüche

1. Verfahren zum Herstellen von Gatestrukturen für einen MOS-Auswähltransistor einer nichtflüchtigen EEPROM-Speicherzelle mit selbstausgerichteten Polysiliziumschichten und einem zugeordneten Schaltungstransistor, mit folgender Abfolge von Schritten:
   a) Aufbringen einer ersten Schicht (4) aus polykristallinem Silizium auf ein zuvor mit Feldoxidbereichen (2) und einer Gateoxidschicht(3) versehenes Substrat (1) aus monokristallinem Silizium;
   b) Definieren und durch Ätzen erfolgendes Entfernen der ersten Polysiliziumschicht (4) auf den Feldoxidbereichen (2);
   c) Aufwachsenlassen einer dünnen Oxidschicht (5) auf der ersten Polysiliziumschicht (4);
   d) durch Ätzen erfolgendes Entfernen der dünnen Oxidschicht (5) zur Bildung eines Fensters (20) in einem zur Bildung des Auswähltransistors bestimmten Bereich (16), wobei das Fenster (20) schmaler ist als die gewünschte Breite der Gatestruktur des Auswähltransistors, sowie durch Ätzen erfolgendes Entfernen der dünnen Oxidschicht über der gesamten Fläche des Schaltungstransistors;
   e) Aufbringen einer zweiten Schicht (11) aus polykristallinem Silizium über der gesamten Struktur;
   f) Aufbringen einer weiteren Oxidschicht (21) über der zweiten Polysiliziumschicht (11);
   g) Anbringen einer Maske (12, 13, 14) auf der weiteren Oxidschicht (21) zum Abdekken von Bereichen (15, 16, 17) zur Bildung der Speicherzelle sowie des Auswähl- und des Schaltungstransistors, wobei der Auswähltransistorbereich (16) das Fenster (9) beinhaltet;
   h) durch Ätzen erfolgendes Entfernen der weiteren Oxidschicht (21), der zweiten Polysiliziumschicht (11) und der dünnen Oxidschicht (5) an den Seiten der Speicherzellen- und Auswähltransistorberei-

che (15, 16), sowie der weiteren Oxidschicht (21), der ersten und der zweiten Polysiliziumschicht (4, 11) und der Gateoxidschicht (3) an den Seiten des Schaltungstransistorbereichs (17) zum Definieren einer Schaltungstransistor-Gatestruktur (17), die durch Bereiche der Gateoxidschicht (3), der ersten und der zweiten Polysiliziumschicht (4, 11) und der weiteren Oxidschicht (21) gebildet wird;

i) Ersetzen der Maske (12, 13, 14) durch eine weitere Maske (22), die den Schaltungstransistorbereich (17) abdeckt;

j) durch Ätzen erfolgendes Entfernen der ersten Polysiliziumschicht (4) an den Seiten der Speicherzellen- und Auswähltransistorbereiche (15, 16) zum Definieren einer Speicherzellen-Gatestruktur (15), die durch Bereiche der Gateoxidschicht (3), der ersten Polysiliziumschicht (4), der dünnen Oxidschicht (5), der zweiten Polysiliziumschicht (11) und der weiteren Oxidschicht (21) gebildet wird, sowie zum Definieren einer Auswähltransistor-Gatestruktur (16), die durch Bereiche der Gateoxidschicht (3), der ersten Polysiliziumschicht (4), der dünnen Oxidschicht (5) mit dem Fenster (20), der zweiten Polysiliziumschicht (11) und der weiteren Oxidschicht (21) gebildet wird.

R vendications

1. Procédé de fabrication de structures de grille pour un transistor MOS de sélection d'une cellule mémoire non volatile EEPROM à couches de silicium polycristallin auto-alignées et pour un transistor du circuit associé, comprenant la succession d'étapes suivantes :

a) déposer une première couche (4) de silicium polycristallin sur un substrat (1) de silicium monocristallin préalablement muni de zones d'oxyde de champ (2) et d'un couche d'oxyde de grille (3) ;

b) définir et enlever par gravure la première couche de silicium polycristallin (4) au-dessus des zones d'oxyde de champ (2) ;

c) faire croître une couche d'oxyde mince (5) sur la première couche de silicium polycristallin (4) ;

d) enlever par gravure la couche mine d'oxyde (5) pour définir une fenêtre (20) dans une zone (16) destinée à la formation du transistor de sélection, la fenêtre (20) étant plus étroite que la largeur souhaitée de la structure de grille du transistor de sélection, et enlever par gravure la couche d'oxyde mince au-dessus de toute la surface du transistor de circuit ;

e) déposer une seconde couche (11) de silicium polycristallin sur toute la structure ;

f) déposer une autre couche d'oxyde (21) sur la seconde couche de silicium polycristallin (11) ;

g) appliquer un masque (12, 13, 14) sur l'autre couche d'oxyde (21) pour recouvrir des zones (15, 16, 17) de formation de la cellule mémoire et des transistors de sélection et de circuit, la zone du transistor de sélection (16) incluant ladite fenêtre (9) ;

h) enlever par gravure l'autre couche d'oxyde (21), la seconde couche de silicium polycristallin (11) et la couche mince d'oxyde (5) au niveau des côtés de la cellule mémoire et des zones (15, 16) du transistor de sélection et de l'autre couche d'oxyde (21), les première et seconde couches de silicium polycristallin (4, 11) et la couche d'oxyde de grille (3) au niveau des côtés de la zone du transistor de circuit (17) de façon à définir une structure de grille de transistor de circuit (17) formée par des parties de la couche d'oxyde de grille (3), les première et seconde couches de silicium polycristallin (4, 11) et l'autre couche d'oxyde (21) ;

i) remplacer ledit masque (12, 13, 14) par un autre masque (22) recouvrant la zone du transistor de circuit (17) ;

j) enlever par gravure la première couche de silicium polycristallin (4) au niveau des côtés de la cellule mémoire et des zones (15, 16) du transistor de sélection de façon à définir une structure de grille (15) de cellule mémoire constituée de parties de la couche d'oxyde de grille (3), de la première couche de silicium polycristallin (4), de la couche d'oxyde mince (5), de la seconde couche de silicium polycristallin (11) et de l'autre couche d'oxyde (21) et une structure de grille de transistor de sélection (16) constituée de parties de la couche d'oxyde de grille (3), de la première couche de silicium polycristallin (4), de la couche d'oxyde mince (5) munie de la fenêtre (20), de la seconde couche de silicium polycristallin (11) et de l'autre couche d'oxyde (21).

Fig.1

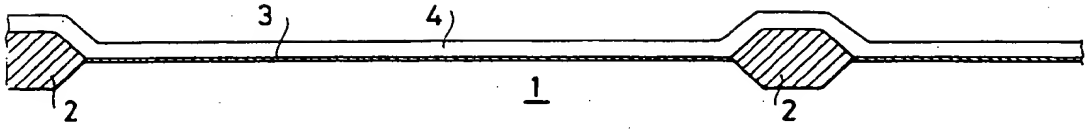

Fig.2

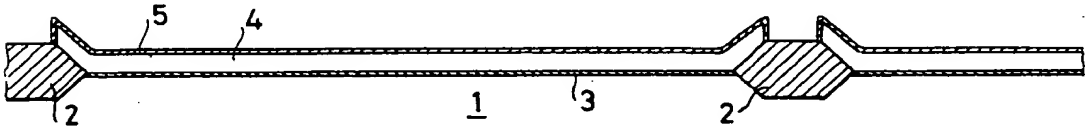

Fig.3

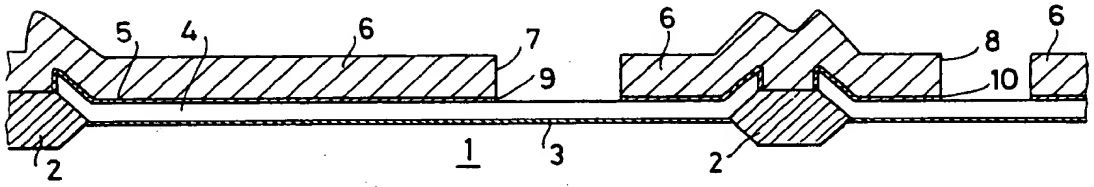

Fig.4

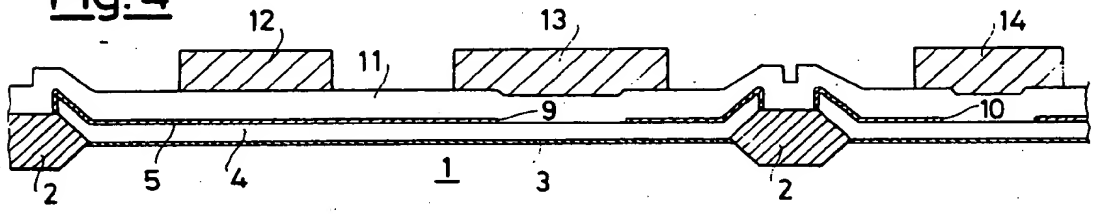

Fig 5

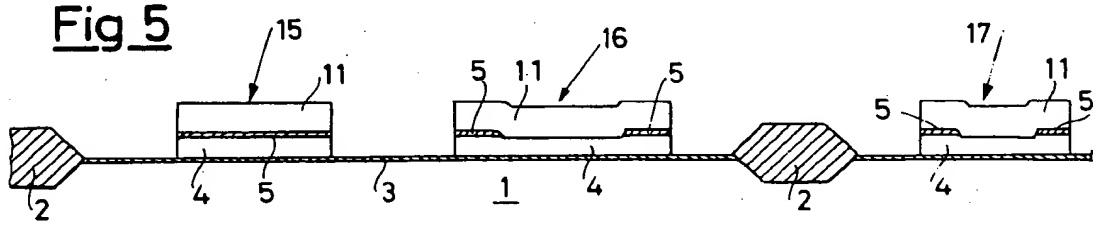

Fig.6

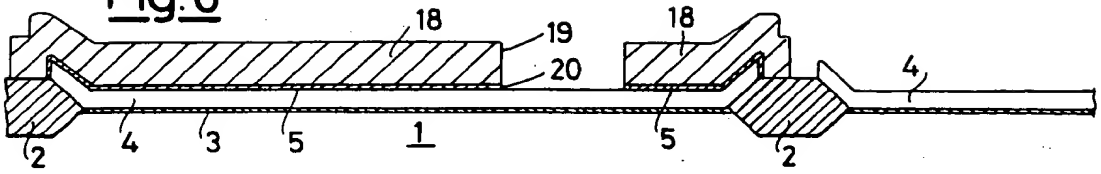

Fig.7

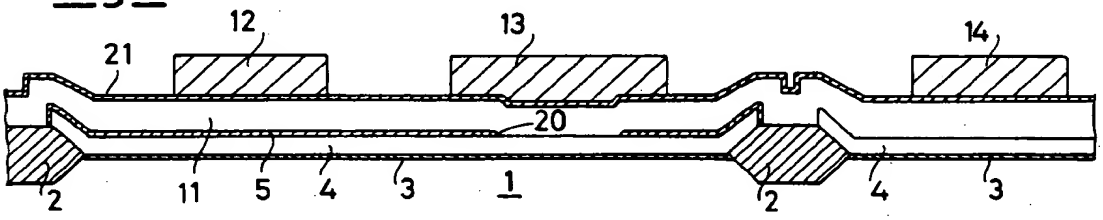

Fig.8

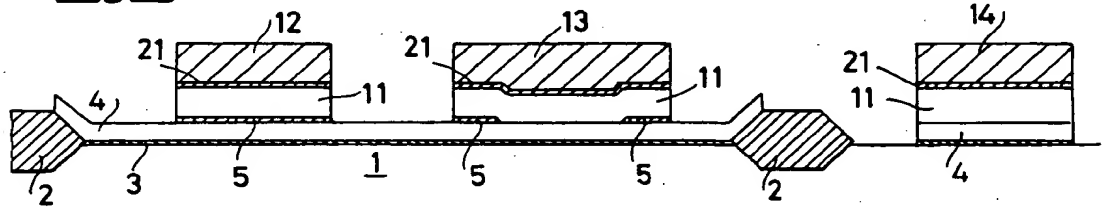

Fig.9

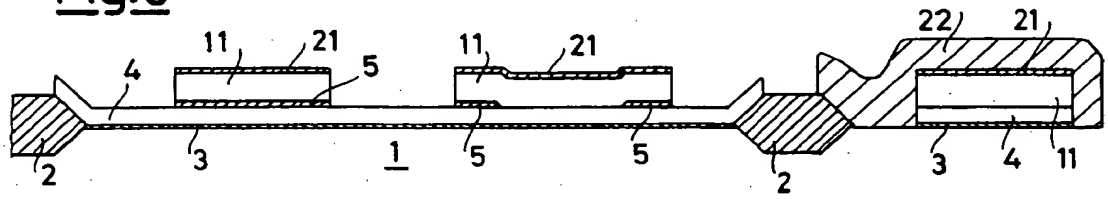

Fig.10

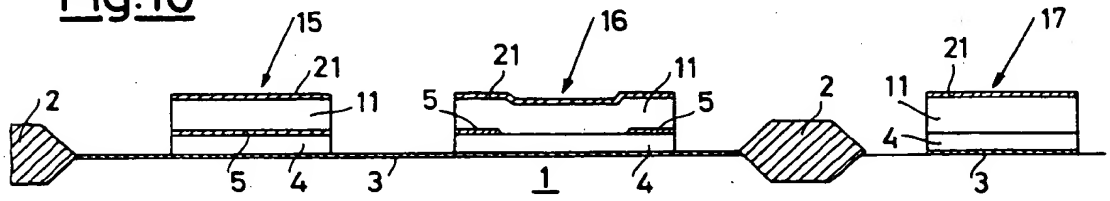

Fig.11

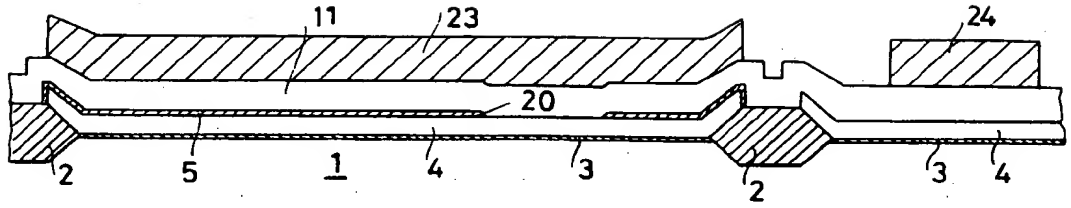

Fig.12

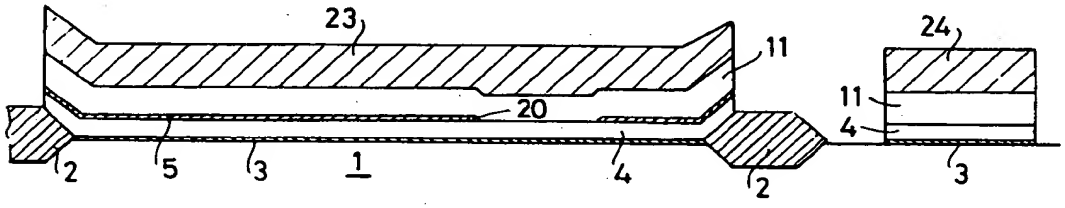

Fig.13

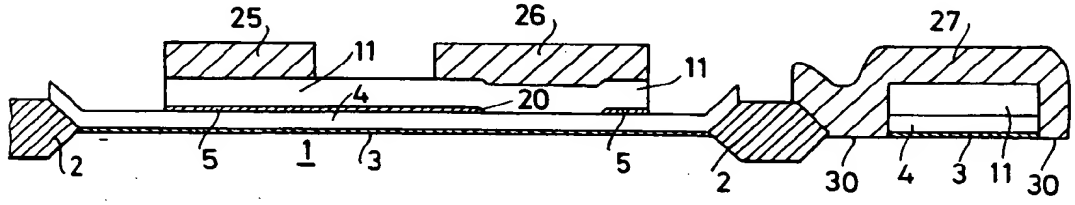

Fig.14